Regulator / Controls for Top-Up Interleaving Power Supplies – Summary of Meetings on 3/22/01 and 3/23/01

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Control requirements for the top-up interleaving power supplies are fairly complex, and involves

- Control of 4 IGBT power switches, at least two of which require independent variable-frequency/variable-duty control.
- Two independent regulator loops, one requiring 100ppm regulation.
- Pulsed vs DC control modes.

Testing of the prototype interleaving power supply will start in July 2001, and three production units must be installed and be operational with APS after the October 2001 shutdown. Control electronics must be provided to support both prototype development and production units.

A separate but related issue is a desire to have a 'cookie-cutter' DSP controller that can be used for various APS projects, but do not involve the expense of existing commercial boards such as those used in the orbit feedback system. Some work has been done towards this for the Power Supply DSP Converter development. Controls Group have prototype high-precision PWM circuit, high-performance 16-bit A/D converter, and a SHARC-based DSP board, all on VME. However, it is the consensus that the Analog Devices SHARC is not a suitable DSP for the 'cookie-cutter' hardware because of limited support, poor compiler performance, and significantly lower through-put than the Texas Instruments C67x DSP.

Implementation options considered for interleaving power supply control

1. Use conventional analog regulator and conventional PWM control, together with Altera implementation of logic control functions.
2. Develop new embedded hardware solution using the Texas Instruments C67x DSP, 16-bit A/D converters, and other I/O functions.
3. Use the evaluation board for the C67x together with a custom daughter card for implementing analog and digital I/O.
4. Use a VME-based solution with existing commercial DSP and A/D boards that have known history at the APS.

All options require custom analog and digital I/O signal conditioning electronics.

Option 1 is relatively low risk, but provides the least flexibility during prototype development, and may not provide the best overall performance. This option gains nothing with regards to the 'cookie-cutter' DSP hardware.

Option 2 would satisfy our goal of having a 'cookie-cutter' solution to DSP applications for future applications. However, there is also some risk in being able to support delivery dates, particularly for July testing.

Option 3 provides the short-term benefit of not having to develop the embedded DSP hardware, but reliability of the evaluation boards is questionable for the long term, and there is still development effort required with the daughter card.

Option 4 probably offers the best chance of supporting prototype development starting in July, but is high cost ($15-20K per unit), and is overkill for this application. It does provide an opportunity to gain further experience with DSP-based software development, but does not get us closer to an embedded solution. If this option were chosen to support July testing, it is not clear how we would progress towards an October delivery date given the high cost of each unit.

A meeting was held on 3/22/01 to discuss these options. In attendance were J. Wang, J.Carwardine, F. Lenkszus, R. Laird, T. Fors, A. Hillman, G. Sprau. At this meeting, an agreement was reached that Option 3 (VME-based solution using commercial hardware) would be pursued for July, an that Lenkszus and Laird would develop a VME-based C67x DSP board, starting in May, with the intention of supporting a less expensive VME-based solution for the production units to be delivered in October.

Subsequent discussions were held on 3/23/01 between J. Wang, T. Fors, J Carwardine, and F. Lenkszus. During these discussions, it was agreed to revise that decision on the basis of the cost of implementing production units in VME ($15-20K per unit), and on the fact that we do not gain the long-term benefit from developing any embedded hardware. The agreement was to approach the problem as follows:

For July:

- Use the evaluation board for C67x DSP, together with a daughter card that contains custom circuits (A/D converters, PWM circuits, and other DSP interfaces).
- Develop an analog and digital interface board between power circuit and DSP.
- Use the evaluation board ‘Host Port Interface” to control the device via a PC computer.
- There will be no IOC support required for the initial testing in July.

For October

- Laird will develop a VME board with C67x DSP that will support future DSP-based needs in VME, and provide the hardware kernel for embedding the C67x DSP for the interleaving power supply controller.
- The C67x hardware kernel will be combined with the A/D converter, PWM circuits, and other interfaces to produce a custom embedded solution.
- IOC communications interface will have to be developed. The implementation of this interface is to yet to be defined.

Preliminary assignment of responsibilities

It is recognized that development of a DSP-based controller, particularly given the timeframe, will require significant effort from staff members of both Controls and Power Supply Groups. A preliminary apportionment of the responsibilities is as follows:

- PS Group will develop the daughter card for the C67x evaluation board, analog and digital interfaces between controller and power circuit, and DSP software.
- Controls Group will develop a VME board with C67x DSP, and will support integration of DSP, A/D converter, PWM circuits, and other interface hardware.
- Controls Group will provide IOC database support.
- Development of the communications interface between IOC and power supply controller is yet to be defined, but is likely to require effort from both Controls and PS Groups.