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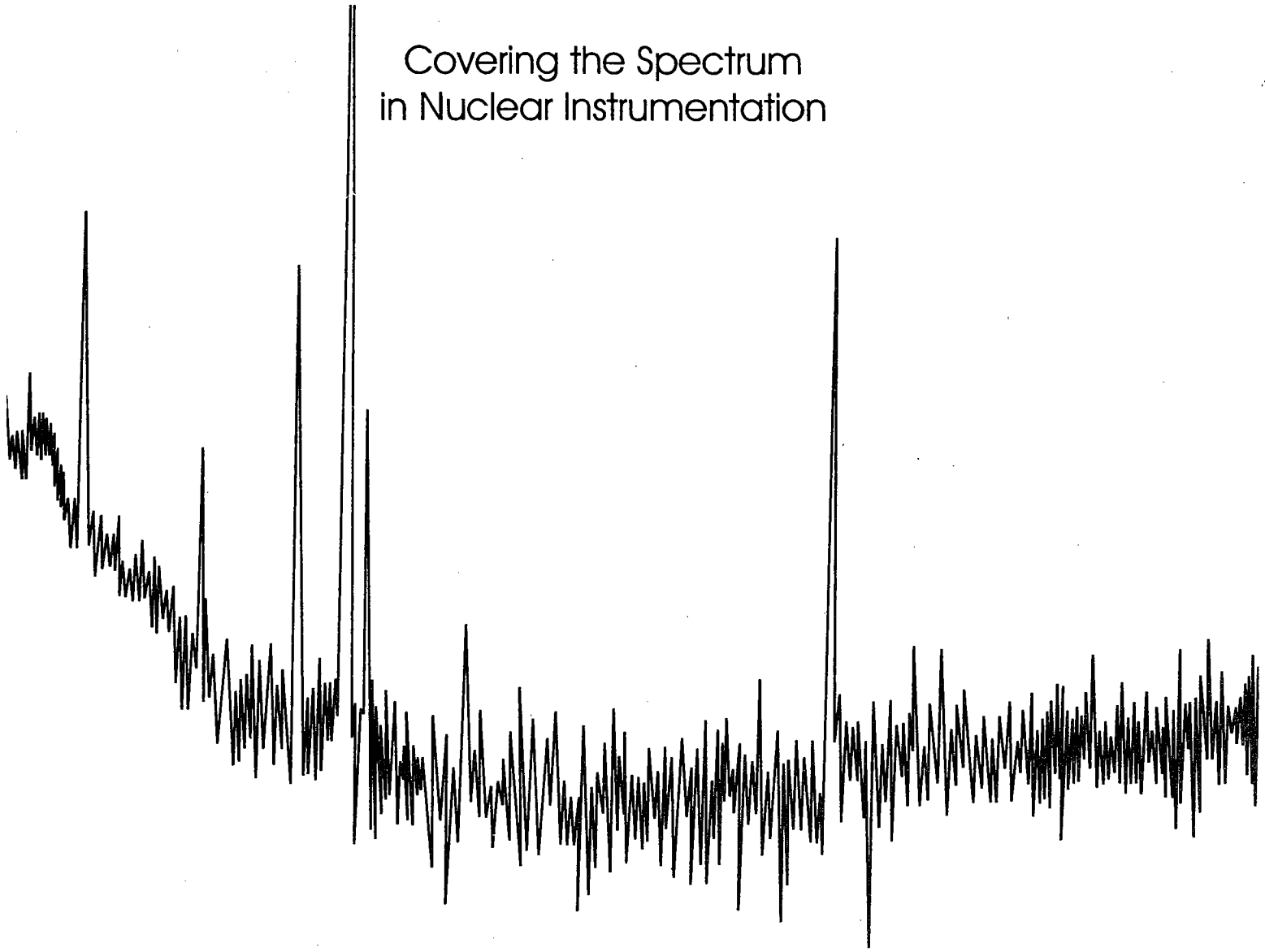
CANBERRA

# Model 2016 Amplifier/TCA

2016-USR 1/98
9231145A

## User's Manual

Covering the Spectrum
in Nuclear Instrumentation



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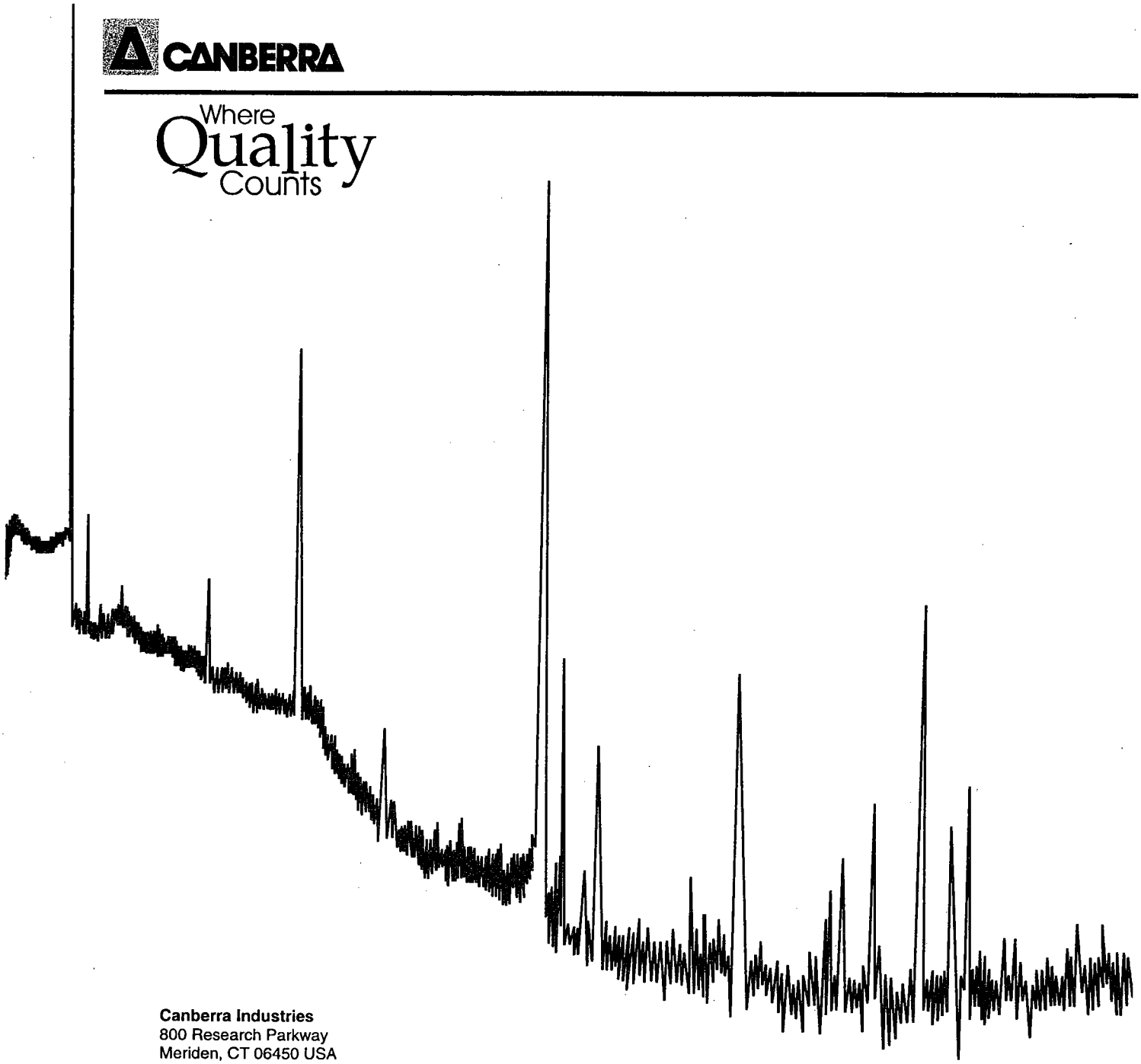


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# Model 2016
# Amplifier/TCA

## User's Manual

2016-USR 1/98
9231145A

ISO 9001
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The information in this manual describes the product as accurately as possible, but is subject to change without notice.

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# 1. Introduction

The 2016 Amplifier-TCA provides the basic signal processing function for x-ray detectors used in high-rate applications such as EXAFS (Extended X-ray Absorption Fine Structure). The Amplifier provides gain, filtering, baseline restoration and ICR pulse discrimination. The TCA provides three computer controlled pulse height (energy) analyzers with selectable pileup rejector and different pulse output options suitable for counting. In addition the 2016 has a built-in multiplexing function which, under computer control, selects the amplifier output and SCA output from each of up to thirty-two 2016's in a system for routing to an MCA (multichannel analyzer) for window set up. All of this capability is in a single-wide NIM allowing large scale systems to be built compactly.

## 1.1 Amplifier Function

The 2016 amplifier is based on the Canberra Model 2025-2026 series of amplifiers which have been used extensively in x-ray and gamma-ray spectroscopy. The shaping time constants have been selected to enhance the throughput rate. The 2016A offers higher throughput rate while the 2016B has longer time constants needed for high resolution at lower rates and for low energy (<1 keV) applications.

| Version | Shaping (μs) |
|---|---|
| 2016A | 1/8, 1/4, 1/2, 1, 2, 3 |
| 2016B | 1/4, 1/2, 1, 2, 4, 6 |

## 1.2 Pulse Height Analyzer Function

The SCA function comprises three independently computer-controlled, single-channel analyzers each of which provides a logic pulse output for each input pulse falling within its preset energy window. Window settings are set using computer control over an Ethernet link to an Acquisition Interface Module (AIM). The AIM to 2016 module interface is accomplished through Canberra's Instrument Control Bus (ICB) for complete control of SCA settings and multiplexed output as described below. For convenience, the window is set symmetrically around a centroid voltage (energy) level. The module's pileup rejector, when enabled by computer, inhibits SCA outputs resulting from input signals that are distorted due to pile-up.

## 1.3 Multiplexer Function

The AIM also provides the Multichannel Analyzer function for set-up purposes when connected to an Analog to Digital Converter (ADC). The 2016's multiplexer function provides signal routing for set-up of each SCA window and normalization of signal levels (gain) using a multichannel analyzer. Typically the "SELECTED AMP" outputs are daisy chained to an ADC signal input and the "SELECTED SCA" outputs are daisy chained to the ADC GATE input. Then, depending on the gate mode chosen, the MCA will either accumulate or exclude only those events falling within the selected SCA window.

## 1.4 ICB Control

Control of SCA settings and selection of multiplexed outputs are accomplished via the ICB from an AIM. The ICB can address up to 16 slave devices from a single AIM which acts as a master. Thus, a typical 13-element detector array system will use a single AIM to address the HVPS, ADC and the required thirteen 2016 TCAs. Implementation of larger systems can be accomplished by adding more AIMs (i.e. a 30-element array will require two AIMs, 30 TCAs, one ADC and one HVPS).

Software to control the setup of the 2016 and other ICB NIM modules is available under Canberra's Genie-2000/Genie-PC and Genie-VMS software packages. Software setup is provided to control the SCA's centroid window on all three SCAs, SCA Polarity Invert, automatic or manual ICR Threshold, SCA select and PUR enable for each SCA. Additionally, the software verifies the instrument serial number and model number each time the input is opened for use.

# 2. Controls and Connectors

## 2.1 Front Panel Controls

This is a brief description of the front panel controls and connectors. For more detailed information, refer to Appendix A, Specifications

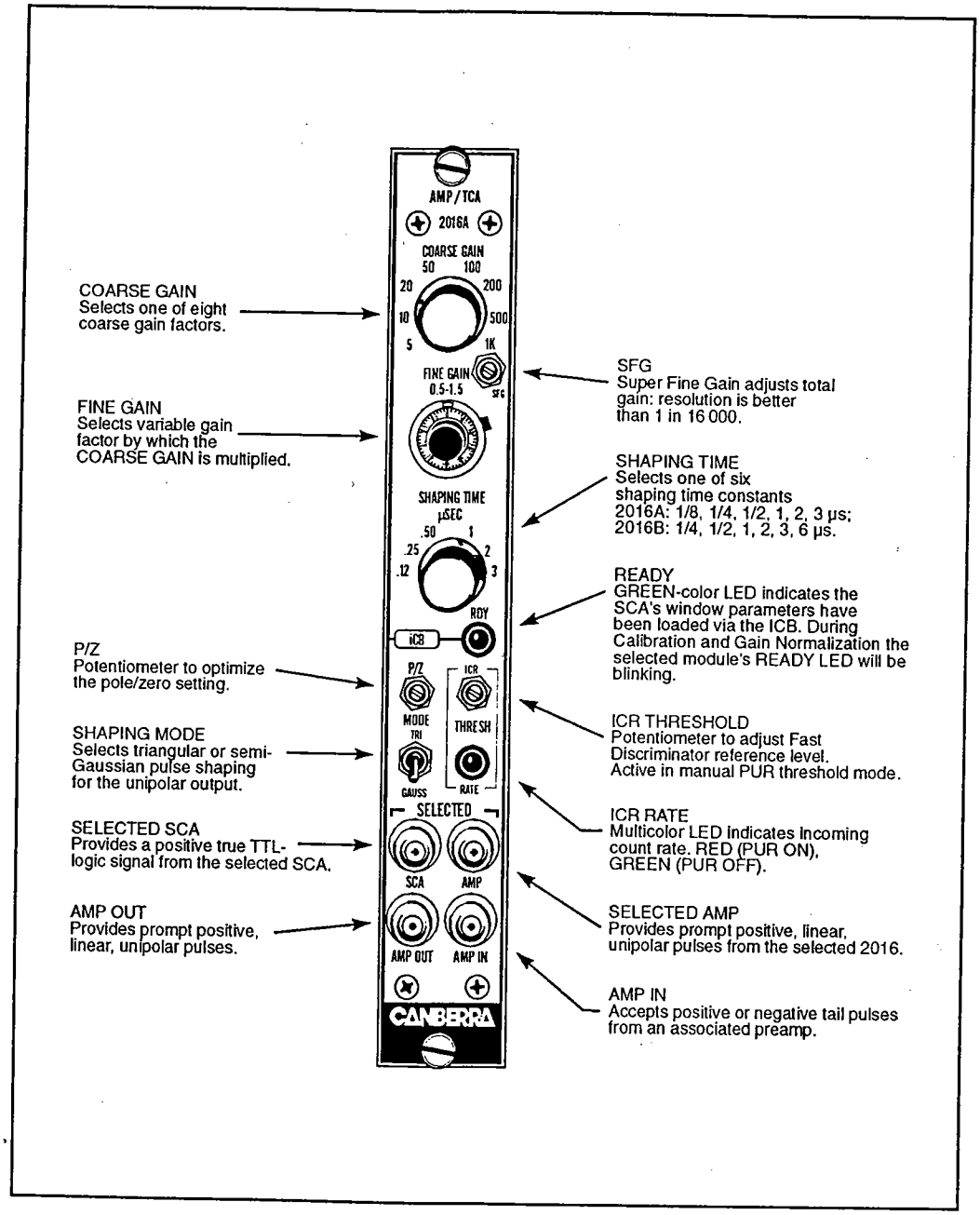



Figure 2.1 Front Panel Controls and Connectors

## 2.2 Rear Panel Connectors

This is a brief description of the rear panel connectors. For more detailed information, refer to Appendix A, Specifications.

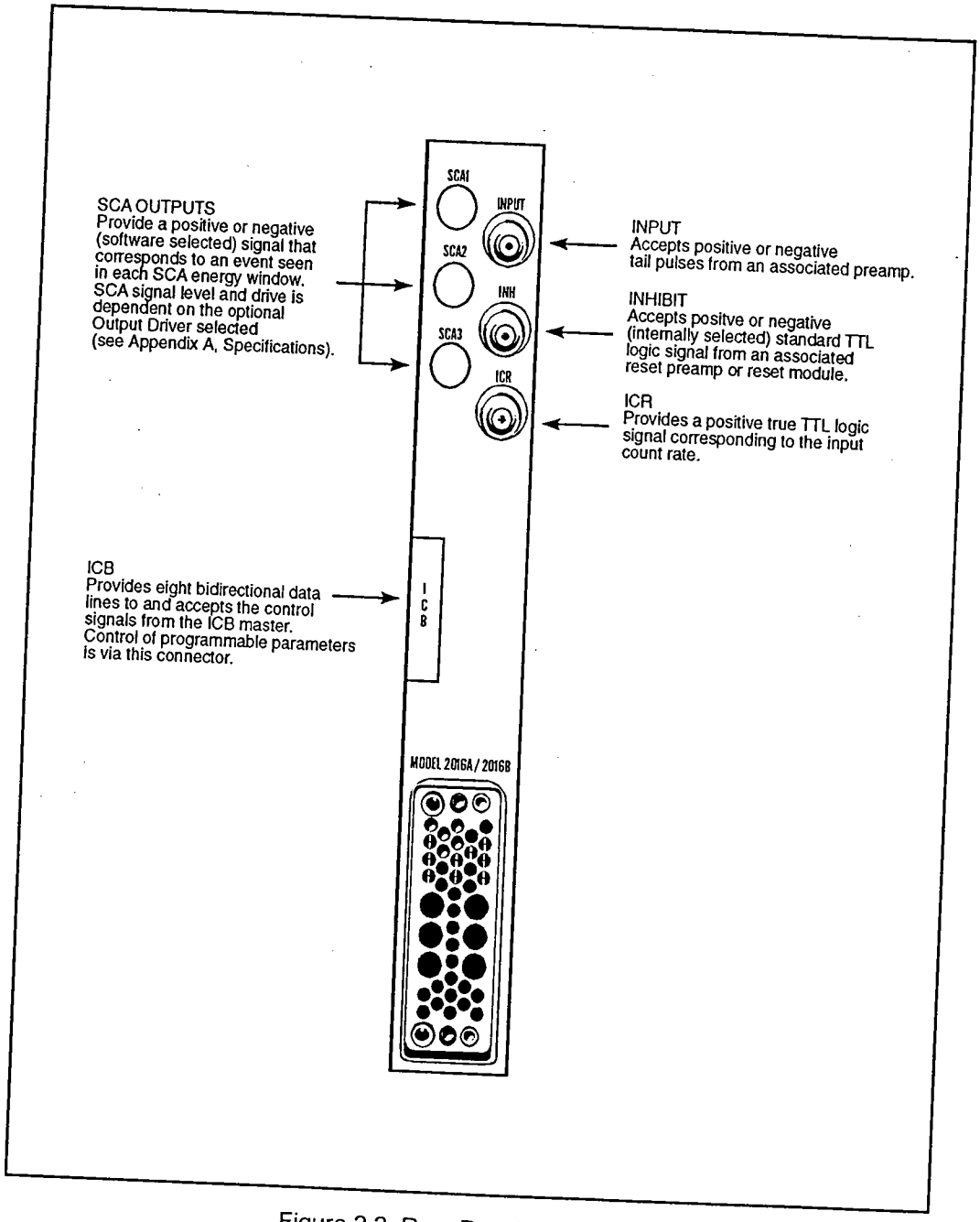



Figure 2.2 Rear Panel Connectors

## 2.3 Internal Controls

### 2.3.1 Amplifier Board

This is a brief description of the jumper controls on the Amplifier board; the jumpers are shown in their factory default positions. For more detailed information, refer to Appendix A, Specifications.

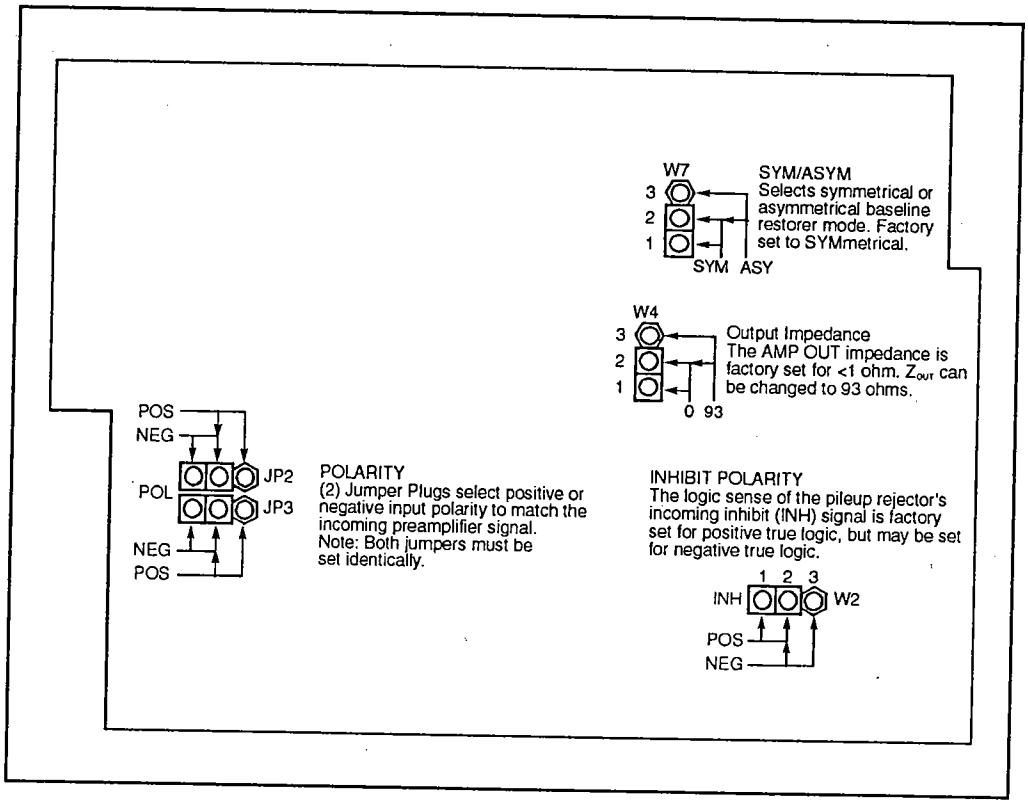



Figure 2.3 Amplifier Board Jumpers

### 2.3.2 TCA Board

The proper DAC voltage range is set at the factory with a jumper in position JP5 or position JP6. For proper operation of this unit, this voltage range jumper must not be moved.

There should be no jumpers installed in positions JP1, JP2, JP3 and JP4; these positions are for factory testing only.

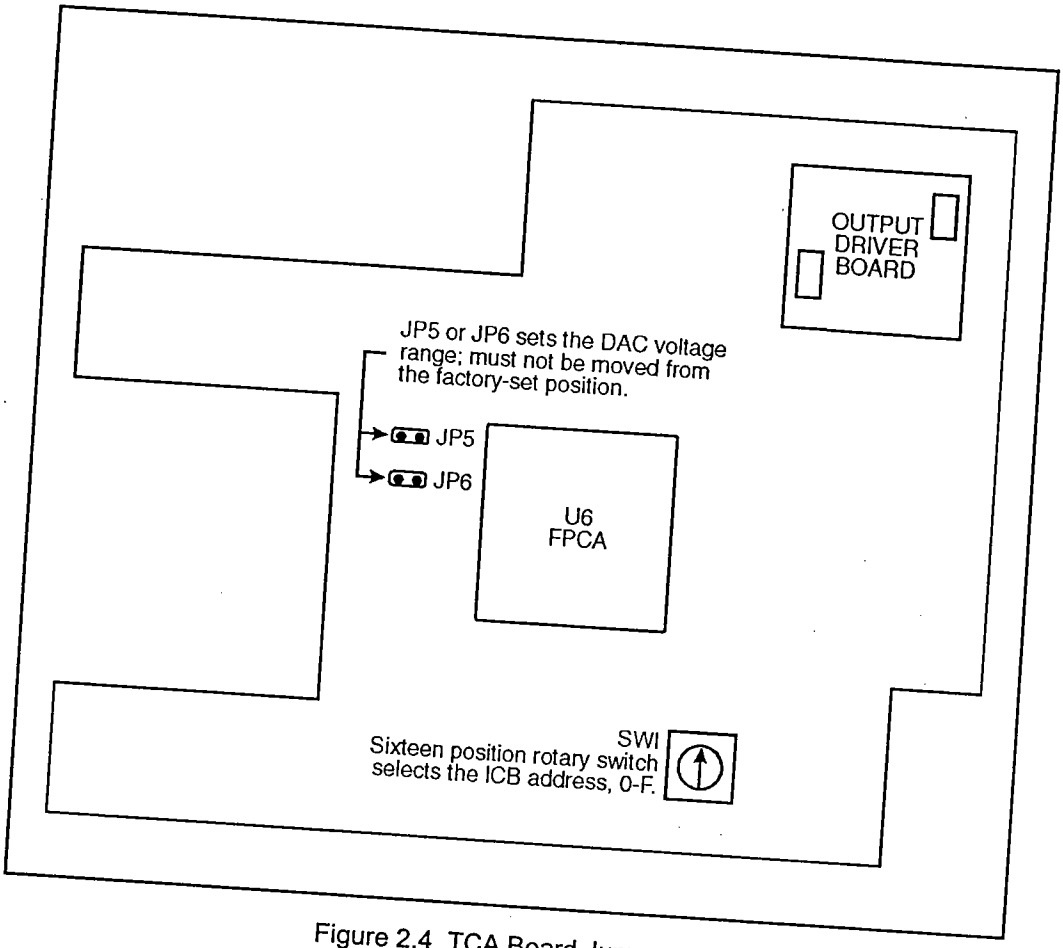



Figure 2.4 TCA Board Jumpers

# 3. Amplifier Operation

This section outlines the operation of the Model 2016 Amplifier-TCA amplifier section. Following these procedures will make you familiar enough with the instrument to be able to use it effectively in any situation.

## 3.1 Hardware Installation

The Canberra Model 2100 Bin and Power Supply, or other bin and power supply systems conforming to the mechanical and electrical standards set by DOE/ER-00457T will accommodate the Model 2016; the module requires ±24 V, ±12 V and ±6 V from the power supply. The right side cover acts as a guide for inserting the instrument. The module is secured in place by turning the two front panel captive screws clockwise until finger tight. It is recommended that the NIM Bin Power switch be OFF whenever the module is installed or removed.

The Model 2016 can be safely operated where the ambient air temperature is between 0 °C and +50 °C (+120 °F max). Perforations in the top and bottom sides permit cooling air to circulate through the module. When relay rack mounted along with other heat generating equipment, adequate clearance should be provided to allow for sufficient air flow through both the perforated top and bottom covers of the NIM Bin.

The standard cable sent with the Model 556 AIM for ICB is the C1560, which allows a total of 11 ICB modules to be controlled by the AIM within one NIM Bin. With array systems, it is desirable to control as many of the 2016 TCAs as possible with each AIM.

With a C1562 cable, the AIM can control up to 16 ICB modules, 11 in one Bin and five in a second Bin. This can be a combination of different modules or all 16 can be 2016 TCAs.

**Caution** Only 2016 modules are designed to operate properly in the extended Bin. Any Model 96xx ICB or Model 554 RPI must be installed in the same Bin as the Model 556 AIM (ICB Master).

## 3.2 Amplifier Setup

Before installing the 2016 in a NIM Bin, its internal controls should be set to their desired positions. When multiple 2016 TCA modules are being used, each must have a different ICB address. Figure 2.4 shows the location of SW1, which sets the module's ICB address.

For a single AIM system, the module's software address (channel number) and hardware ICB address (determined by SW1) are:

$$(\text{channel number})_{10} \doteq (\text{ICB})_{16} + 1$$

or

$$1 \rightarrow 16 \doteq 0 \rightarrow F + 1$$

When more than 16 modules are required, two AIMs are needed. The addresses from the first AIM which would also include other non-Amplifier/TCA modules, such as an ADC or HVPS, are still in the range of 1 → 16, corresponding to the ICB switch positions of 0 → F. Any non-ICB ADC (such as the Model 8715), must also be connected to the first AIM. All Amplifier/TCAs on the second AIM's Control Bus are channel numbered 17 → 32, corresponding to ICB switch positions 0 → F.

1. Insert the Model 2016 into a standard NIM Bin. Allow the total system to warm up and stabilize for approximately 15 minutes.
2. Set the Model 2016 controls as follows:

   SHAPING TIME . . . . . 0.5 μs
   MODE . . . . . Gaussian
   COARSE GAIN . . . . . 1K
   FINE GAIN . . . . . 10

3. This will give approximately an 8 volt output when using a preamp with a gain of 100 mV/MeV and a $^{55}Fe$ radioactive source.

## 3.3 Preamp Fall Time Matching

Pole/zero compensation is critical when using resistive feedback preamplifiers. Pole/zero compensation must be readjusted whenever the shaping time is changed or when the 2016 is connected to a different detector. Refer to "Pole/Zero Matching" on pages 31 and 32 for instructions on adjusting the pole/zero compensation.

When a reset type preamp is used, pole/zero compensation is not required and the control must be set fully counterclockwise (infinity).

# 4. Operation With ADC and MCA

Figure 4.1 shows a typical array detector system configured for 2016 Amplifier/TCA calibration and operation. Each Preamp output is connected to a 2016 Amp Input. SCA parameters are computer controlled through the Model 556 AIM, utilizing Canberra's Instrument Control Bus (ICB). All 2016 Selected SCA Outputs are connected to an ADC Gate Input. The 2016 Selected Amp Output is connected to an ADC Input. With the ADC configured for Delayed Peak Detect, the 2016 Selected SCA controls ADC conversion, allowing calibration of each 2016 Amplifier/TCA. When calibrating each 2016 Amplifier/TCA module, its SCA energy window is set up and SCA count analysis can begin.

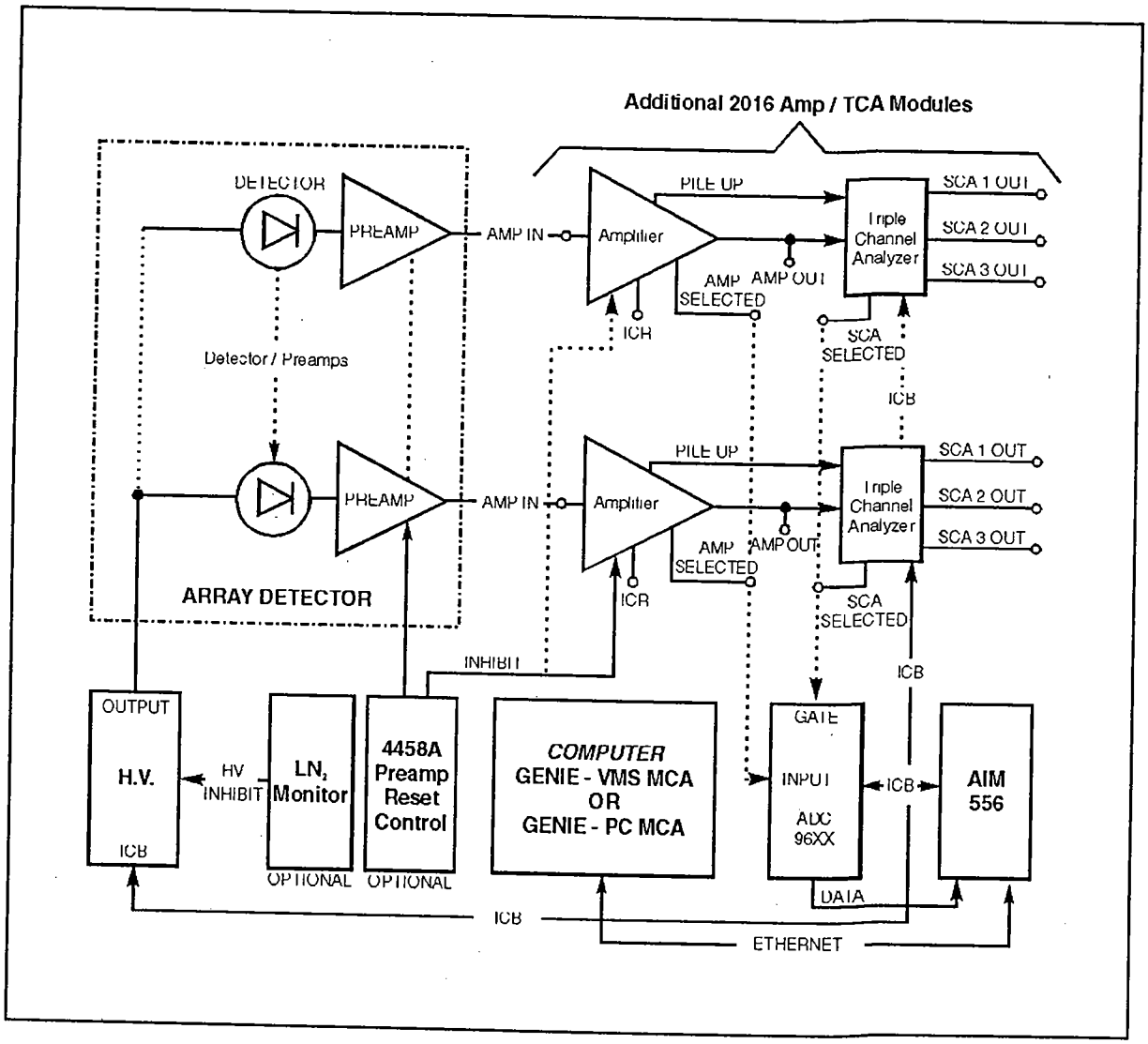



Figure 4.1 Typical 13-Element Array Detector System

## 4.1 ADC Setup

Please refer to your ADC user's manual for specific ADC operating instructions.

Set the ADC's GAIN and RANGE equal to the MCA memory group size. For instance, set the GAIN and RANGE to 4096 for an MCA with a 4096 channel memory size.

Set the ADC controls to:

LLD . . . . . 0.02 V (fully counterclockwise)
ULD . . . . . 10.5 V (fully clockwise)
Digital Offset . . . . . All Off
Peak Detect . . . . . Delayed

With a low count rate, use the ADC's Inspect test point to set the ADC's Peak Detect Delay to be greater than the SCA's Output pulse. Refer to "ADC Peak Detect Adjustment" on page 37 for the procedure to be followed.

## 4.2 Spectroscopy Operation

Please refer to your MCA user's manual for specific MCA operating instructions.

Start acquiring data in the MCA using the $^{55}Fe$ radioactive source previously placed near the detector. A spectrum should begin to appear on the MCA's display.

Adjust the Amplifier's GAIN so that spectrum is positioned conveniently on the display.

Use the Amplifier's Super Fine Gain (SFG) when matching gains of other detectors, or when establishing a specific gain (energy per channel). This control provides 100 times more resolution than the Fine Gain Control.

# 7. Circuit Description

## 7.1 Amplifier

The 2016 amplifier includes a differential input stage for polarity selection, followed by a differentiator, three low noise gain amplifier stages, three complex-pole active-filter stages (optimized for improved pulse symmetry), a gated active baseline restorer and a unipolar output amplifier providing semi-Gaussian or semi-triangular output pulse shaping. A bipolar stage is provided for SCA timing.

### 7.1.1 Input Amplifier

Gain amplifier 1 (schematic sheet 1) is a discrete low noise differential amplifier comprised of transistors Q1 through Q5, Q7, Q28 and Q29. This amplifier's gain is selected by the coarse gain switch and relay K1 and is X1 for a coarse gain of 5 and X2 for coarse gains of 10 and higher. Polarity is selected by having the input signal drive Q29(+) or Q28 (–). The negative-going output signal provided by this stage drives the pole/zero circuit and the first differentiator.

### 7.1.2 Differentiator and Gain Stages

The input amplifier's output signal is differentiated by C13 through C18A and resistor R25 (schematic sheet 2). The pole/zero compensation is performed by potentiometer RV3 and resistors R45 through R49 and R26. The time constants are selected by sections of the shaping switch.

The differentiated and pole/zero compensated signal is amplified by gain AMPs 2 (A1), 3 (A2) and 4 (A3) or gain AMPs 2 and 4, depending on the COARSE GAIN switch selection (schematic sheets 1 and 3). FINE GAIN and SFG (Super Fine Gain) are performed in concert with gain AMP 2 and potentiometers RV8 and RV1 respectively. The gain adjustment range of gain AMPs 2 through 4 are continuously adjustable from X2.5 to X750. Limiters in the feedback path of each amplifier eliminate op-amp saturation maintaining good overload recovery. The output signal of gain AMP 4 is normally negative and drives the FAST DISCriminator circuits and active integrators A4, A5 and A6

### 7.1.3 Gain Stage Stabilizer

A dc stabilizer (schematic sheet 2) is provided around the gain stage amplifiers to maintain the dc output at gain AMP 4 near zero volts over a wide range of temperatures and count rates. Transconductance amplifier A23 monitors the output of gain AMP 4 with respect to zero volts and generates a correction voltage that is summed in at the input of gain AMP 2. The stabilization loop time constant is determined by the transconductance current programming resistors R14 and R276 and capacitors C2 and C26 resulting in a time constant sufficiently long so as not to have an effect on the overall amplifier shaping transfer function.

### 7.1.4 Active Filters

Three active filter stages, A4, A5 and A6 (schematic sheet 4), produce complex pole pairs providing a near Gaussian pulse shape and a sharp cutoff frequency characteristic for optimal signal to noise ratio. The filter time constant is selected by the shaping switch and associated resistors and capacitors. The output signal from the third integrator is normally negative and drives the unipolar output amplifier.

### 7.1.5 Unipolar Output

The signal provided by the third complex pole integrator drives the unipolar output amplifier (schematic sheet 5) and associated driver, A8 and transistors Q21, Q22 and Q31. The unipolar output amplifier includes a single pole filter provided by feedback resistor R163 and capacitors C81 through C86; the time constant is selected by the shaping switch. For Gaussian shaping the unipolar output provides a semi-Gaussian pulse shape. However, if the triangular shaping is selected, relays K2 and K3 are activated which allow the signals from complex pole integrators A4, A5, and A6 to be summed at the input of the unipolar output amplifier, in the correct proportion, producing a semi-triangular output signal.

### 7.1.6 Baseline Restorer

The baseline restorer (schematic sheet 5) maintains the unipolar output signal baseline at ground reference, with precision, over a wide range of count rates. Transconductance amplifier A10 monitors the unipolar output signal and develops a correction voltage, having the correct amplitude and polarity, which is summed at the input of the unipolar output amplifier to reference the unipolar output signal baseline at zero volts. The baseline restorer is gated and operates only in the absence of or in between output pulses providing superior baseline control over a very wide range of count rates.

Restorer symmetry is selectable is selectable by ASYM/STM jumper plug W7. For the symmetrical restorer mode, positive and negative restoration slew rates are equal. When the asymmetrical is selected, the negative restorer slew rate is reduced substantially providing a softer restorer response for positive output signals

### 7.1.7 Restorer Gate, Auto Threshold and Auto Rate

Baseline correction (schematic sheet 6) is prevented during unipolar output signal intervals that exceed the baseline restorer threshold. Comparators A11A and A11B monitor the unipolar output signal and disable or gate off the baseline restorer for signals that exceed the automatic positive or negative threshold.

The auto baseline restorer threshold circuit, comprised of A9 and A24, peak detects the negative noise excursions of the unipolar output signal and generates a positive dc reference voltage equal to the average value of the unipolar output noise level. This voltage serves as the baseline restorer gating reference that maintains precision for a wide range of amplifier conditions and applications.

Transistors Q14, Q16, capacitor C92 and the baseline restorer gate signal (PBLR) produce a voltage reflecting the count rate (schematic sheet 5). This voltage in turn determines the correction rate of the baseline restorer.

### 7.1.8 Fast Discriminator

A Fast Discriminator circuit (sheet 6) is included to monitor the input events. This provides an output (ICR) to ratemeters as well as a visual indication of count rate given by a front panel LED. The SCA uses the output from the Fast Discriminator (FDO) to determine if multiple inputs are received during a pulse processing sequence. If pileup reject (PUR) is enabled, the SCA outputs are inhibited when pileup occurs.

The signal from AMP 4 is differentiated and pole/zero compensated before being amplified by A34. Amplifier/limiter A34 is baseline restored by transconductance amplifier and gating

transistors Q36/Q37. The discriminator A21 generates a short timing pulse whenever the fast signal from A34 exceeds the threshold level.

This threshold level can be set automatically or manually by using a front panel adjustment. The AUTO threshold circuit (A20 and A22) peak detects the negative-going noise level and uses this absolute value for the threshold. Its operation is similar to the BLR threshold circuit described in "Restorer Gate, Auto Threshold and Auto Rate" on page 23.

### 7.1.9 Bipolar Amplifier and Crossover Timing

The signal from integrator stage 3 is differentiated, producing a bipolar signal at A7 (sheet 8). The shaping time constant is selected by a section of the shaping switch.

The crossover time when this bipolar signal goes negative provides a consistent reference point after the peak of the unipolar output. Comparator A37 turns this into a negative-going logic pulse for the SCA logic.

### 7.1.10 Inhibit Input

This input is usually generated during the recovery time associated with TRP or optical reset preamplifiers. During its active pulse width, the automatic threshold determining circuits, the baseline restorer and all SCAs are gated off.

## 7.2 Triple Channel Analyzer

### 7.2.1 Computer Controlled Logic

Computer control of the Triple Channel Analyzer (TCA) is provided by the Field Programmable Gate Array (FPGA) U6 and three dual DACs U7, U8 and U9. U6 provides the interface to the ICB and contains the registers required to hold the configuration of the SCA.

U3 is a nonvolatile RAM which contains the module Type ID and module serial number.

SW1 is a 16-position binary-encoded rotary switch which sets the module's ICB address.

U7 through U9 are dual 12-bit serial DACs whose output are the LLD and ULD levels that determine each SCA energy window. These DACs are loaded by the FPGA with values it receives from the ICB. Each dual-DAC is loaded by sending it 24 clock pulses (SCLK) that shift in a data code on DIN; the accompanying chip select (CSn*) determines which of the three dual-DACs is loaded.

The DAC reference voltage (–3.5 volts) is obtained using a precision reference in a Zener diode configuration. Jumpers JP5, JP6 and RV1 select and adjust the DAC reference voltage.

### 7.2.2 SCA Front End

Input pulse discrimination is accomplished using six high speed comparators U10 through U15. Three precision voltage dividers in parallel split and scale the unipolar input pulse to be compatible with the DAC reference level. Comparators U10, U12, and U14 (schematic sheet 2) discriminate between the scaled unipolar signal and upper reference level (ULD) producing

a TTL positive logic level when the unipolar signal is above the ULD level. U11, U13 and U15 (schematic sheet 2) discriminate between the scaled unipolar signal and lower reference level (LLD) producing a TTL positive logic level when the unipolar signal is above the LLD level.

### 7.2.3 SCA Logic

The FPGA uses the signals from the LLD and ULD comparators to determine if an input pulse satisfies any of the windows set for the three SCAs. The logic can most easily be described by the timing diagram in Figure 7.1. If an input causes an LLD crossing without a subsequent ULD detection before the peak is signalled, an SCA pulse can be generated.

An important point to note is that as count rates increase, it is likely that some pulses may not cause an LLD crossing because the previous pulse has not fallen below the LLD threshold; for this reason, the pulse shaping must be set consistent with the input count rate. As noted earlier, the peak signal is derived from the bipolar shaping amplifier and give a timing reference after the peak of the unipolar signal.

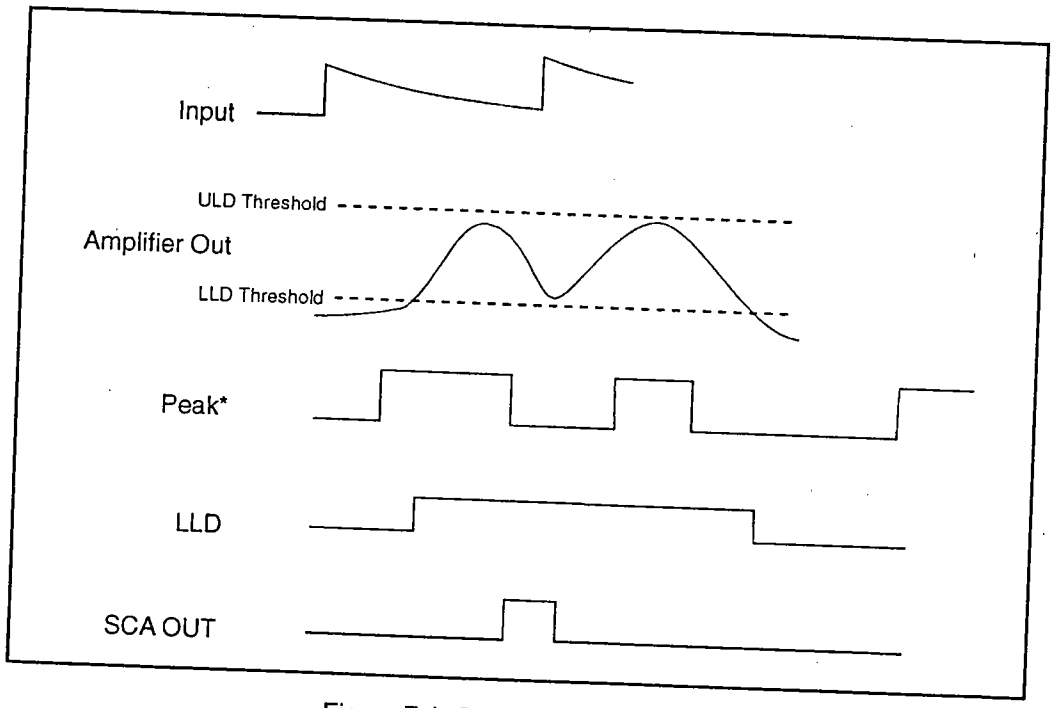



Figure 7.1 SCA Timing Diagram

### 7.2.4 Pileup Rejector

As count rates increase, the possibility of peak pileup, a peak's amplitude being distorted by a succeeding pulse, increases. PUR logic, which can be enabled through the computer interface, will prevent SCA outputs if there is peak pileup. With this logic enabled, the outputs of the Fast Discriminator, and the LLD, ULD and Peak signals are used. Figure 7.2 illustrates the various possibilities. As explained in the previous section, for an SCA signal to be generated,

there must be an LLD crossing, then a Peak detection without a ULD. Assuming that all of the inputs meet these prior conditions:

1. Peak signals 1 and 2 will cause an SCA pulse because there was only a single Fast Discriminator pulse between them.
2. Peak Signal 3 will *not* generate an SCA pulse because more than one FDO was recorded between peaks 2 and 3.
3. Peak 4 shows the condition when multiple inputs are received but cannot be resolved by the Fast Discriminator circuits. This results in a single FDO and an SCA.

Implicit to this discussion is that the Reject logic is initialized (cleared) shortly after the PEAK* edge, as shown in the timing diagram in Figure 7.2.

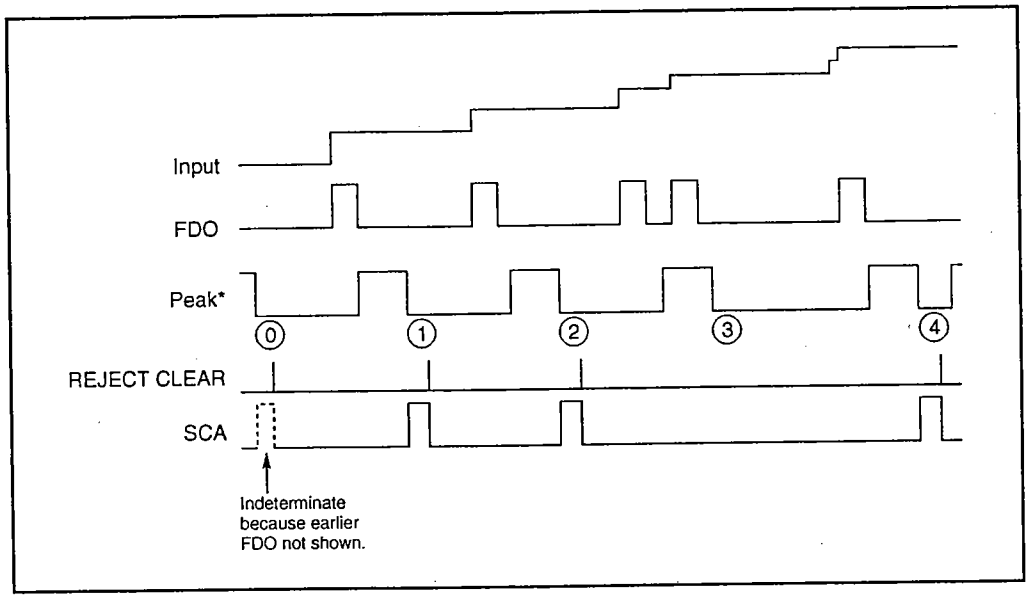



Figure 7.2 PUR Timing Diagram

### 7.2.5 SCA Output Drivers

The logic pulses developed in the FPGA are brought through a plug-in buffer board. Three types of boards can be inserted in the 2016:

- Fast NIM (negative pulse).
- TTL.
- TTL with 50 Ω drive.

# A. Specifications

## A.1 Inputs

INPUT - Accepts positive or negative tail pulses from an associated preamplifier; amplitude 10 V divided by the selected gain, 25 V maximum; rise time: less than shaping time constant; decay time constant: 40 μs to ∞; polarity set with internal jumpers; $Z_{in}$ 2 kΩ > $Z_{in}$ > 0.5 kΩ, depending on input POLARITY and COARSE GAIN; front and rear panel BNC connectors.

INHIBIT - Accepts a standard TTL logic signal from associated reset preamplifier; used to inhibit the SCAs and reset the pileup rejector during the preamplifiers reset cycle; positive true or negative true signal polarities, internal jumper plug selectable; loading: 4 kΩ resistor connected to +5 V for positive true or ground for negative true; rear panel BNC.

## A.2 Outputs

AMP OUT - Provides positive, linear, actively filtered shaped pulses; amplitude linear to +10 V, 12 V max.; dc restored; dc level factory calibrated to 0.5 mV; $Z_{out}$ = <1 Ω or 93 Ω, internally selectable; short circuit protected; front panel BNC.

SELECTED AMP - Provides positive computer selected, linear, actively filtered shaped pulses; amplitude linear to +10 V, 12 V max.; dc restored; output dc level factory calibrated to 0.5 mV; $Z_{out}$ = 93 Ω; short circuit protected; front panel BNC. Computer determines if SELECTED AMP OUTPUT is active.

SELECTED SCA - Provides a standard positive TTL logic output signal coincident with computer's selection of SCA one, two, or three; pulse width 0.1 μs, nominal; rise time and fall time <25 ns; $Z_{out}$ = 51 Ω; 6mA drive capability for TTL high or low level; front panel BNC.

ICR - provides a standard positive TTL logic signal corresponding to input count rate; disabled by INHIBIT; positive true; width nominally 150 ns, TTL with 1 kΩ pull up resistor through 47 Ω output resistor; rear panel BNC.

SCA 1, 2, or 3

Fast NIM Option - Provides negative current output -16 mA into 50 Ω; rise time < 5 ns; pulse width <0.1 s; rear panel EPL00-250NTN LEMO connector.

TTL Option - Provides positive logic +5 V nominal pulse level; pulse width <0.1 μs; rise and fall times <25 ns; rear panel EPL00-250NTN LEMO connector.

50 Ω TTL Option - Provides positive logic +5 V nominal pulse amplitude; $Z_{out}$ = 50 Ω; pulse width <0.1 μs; rise and fall times <25 ns; rear panel EPL00-250NTN LEMO connector.

## A.3 Indicators

ICB READY - Green LED; on steadily indicates that the TCA parameters are loaded and active; blinking indicates that the selected SCA is active.

ICR RATE - Multi-colored LED; Red indicates that PUR is on; Green indicates that the PUR is off; the LED's intensity is count rate dependent.

## A.4 Pileup Rejector

PULSE PAIR RESOLUTION - 250 ns.

MINIMUM DETECTABLE SIGNAL - Limited by detector/preamp noise characteristics.

PUR Threshold - Auto or Manual Adjust mode; computer selectable.

PUR Enable - On or Off; computer selectable.

## A.5 Internal Jumpers

RESTORER MODE - Two-position internal jumper selects SYMmetrical or ASYMmetrical baseline restorer modes; factory set to SYMmetrical.

POLARITY - Two 2-position internal jumpers must be set identically to select INPUT polarity; factory set to negative.

INHIBIT POLARITY - Two-position internal jumper selects INHIBIT input polarity, positive or negative true; factory set to positive.

AMP OUT IMPEDANCE - Two-position internal jumper selects $Z_{out}$ <1 Ω or 93 Ω; factory set to <1 Ω.

## A.6 Manual Controls

COARSE GAIN - Eight-position rotary switch selects gain factors of x5, x10, x20, x50, x100, x200, x500, x1000.

FINE GAIN - Ten-turn locking dial precision potentiometer selects variable gain factor of x0.5 to x1.5; resettability = 0.03%.

SFG (Super Fine Gain) - Multi-turn screwdriver potentiometer adjusts fine gain with a resolution of better than 0.0063%.

P/Z (Pole/Zero) - Multi-turn screwdriver adjustable pole/zero matching potentiometer optimizes amplifier baseline recovery and overload performance for the preamplifiers fall time constant and the amplifiers chosen shaping time; range: 40 μs to ∞.

SHAPING MODE (2016A) - Six-position rotary switch provides 0.125, 0.25, 0.5, 1, 2, and 3 μs shaping time constant.

SHAPING MODE (2016B) - Six-position rotary switch provides 0.25, 0.5, 1, 2, 4, and 6 μs shaping time constant.

ICR THRESH - Multi-turn screwdriver potentiometer adjusts PUR threshold to optimize pile-up selection; active in manual PUR threshold mode.

## A.7 Computer Controls

SCA Window centroid and width; PUR enable/disable; TCA enable/disable and polarity; PUR threshold auto/manual.

## A.8 Performance

GAIN RANGE - Continuously variable from x2.5 to x1500.

TEMPERATURE STABILITY - AMP OUT Gain: 0.005%/°C, dc level: 7.5 V/°C.

INTEGRAL NONLINEARITY - 0.04% over total output range for 2 μs shaping.

OVERLOAD RECOVERY - AMP OUT output recovers to within 2% of full scale output from x1000 overload in 2.5 non-overloaded pulsewidths at full gain, at any shaping time constant, and with P/Z properly set.

PULSE SHAPING - Near-Gaussian or near-triangular shape; one differentiator; three active filter integrators realizing eight-pole shaping network.

RESTORER - Active gated.

SCA NONLINEARITY - <0.25% of full scale.

SCA STABILITY - <±0.005%/°C (50 ppm/°C) of full scale.

SCA RANGE - 1000:1.

SCA PULSE PAIR RESOLUTION - <250 ns using 0.125 μs shaping.

## A.9 Power Requirements

| | | |
|---|---|---|
| +24V dc - 100 mA | +12 V dc - 175 mA | +6 V dc - 350 mA |
| –24 V dc - 120 mA | –12 V dc - 130 mA | –6 V dc - 200 mA |

## A.10 Physical

SIZE - Standard single-width NIM module 3.43 x 22.12 cm (1.35 x 8.71 in.) per DOE/ER-00457T.

NET WEIGHT - 1.5 kg (3.3 lb).

SHIPPING WEIGHT - 2 kg (4.4 lb).

## A.11 Environmental

Operating Temperature Range - 0 to 50 °C.

Humidity - Up to 95% non-condensing.

## A.12 Ordering Information

| MODEL | SCA Output | SHAPING |
|---|---|---|
| 2016A-1 | Fast NIM Driver | 0.125 μs -3.0 μs |
| 2016A-2 | TTL | 0.125 μs - 3.0 μs |
| 2016A-3 | TTL 50 Ω | 0.125 μs - 3.0 μs |
| 2016B-1 | Fast NIM Driver | 0.250 μs - 6.0 μs |
| 2016B-2 | TTL | 0.250 μs - 6.0 μs |
| 2016B-3 | TTL 50 Ω | 0.250 μs - 6.0 μs |

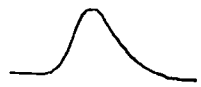
# B. Performance Adjustments

At high count rates, the pole/zero (P/Z) matching adjustment (compensation) is extremely critical for maintaining good resolution and low peak shift. For a precise and optimum setting of P/Z matching, a scope vertical sensitivity of 50 mV/div should be used.

With correct P/Z, spectral peaks will appear symmetrical.

Undercompensated P/Z will produce low energy tailing.

Overcompensated P/Z will produce high energy tailing.



Higher scope sensitivities can also be used, but result in a less precise P/Z matching adjustment. However, most scopes will overload for a 10 V input signal when the vertical signal returns to the baseline. Thus the P/Z matching will be incorrectly adjusted resulting in a loss of resolution at high count rates.

When performing the following manual P/Z matching adjustments, set the scope's vertical sensitivity to 50 mV/div and use a clamp box, such as the Canberra Model LB1502 Schottky Clamp Box, to view the unipolar signal. This will eliminate potential scope overload, and allow precise manual P/Z matching adjustment.

## B.1 Pole/Zero Matching Using an Ultra LEGe Detector and $^{55}$Fe.

1. Set the gain for a Unipolar Output signal of 8 to 10 volts.
2. Adjust the $^{55}$Fe source count rate to be between 2 kcps and 25 kcps.
3. Using a clamp box, such as the Canberra Model LB1502 Schottky Clamp Box, observe the AMP OUT signal on the scope and adjust the manual P/Z control so that the trailing edge of the unipolar pulse returns to the baseline with no overshoots or undershoots.

Figure B.1 shows the correct setting of the P/Z control. Figures B.2 and B.3 show under- and over-compensation for the preamplifier decay time constant. As illustrated in Figure B.1, the AMP OUT signal should have a clean return to baseline with no bumps, overshoots or undershoots.

Note Using a reset preamplifier the P/Z control is adjusted fully CCW. Some amplifier shapings might exhibit small undershoots. These arise primarily from amplifier shaping component tolerances and secondary time constants associated with the detector/preamp system. If an under-

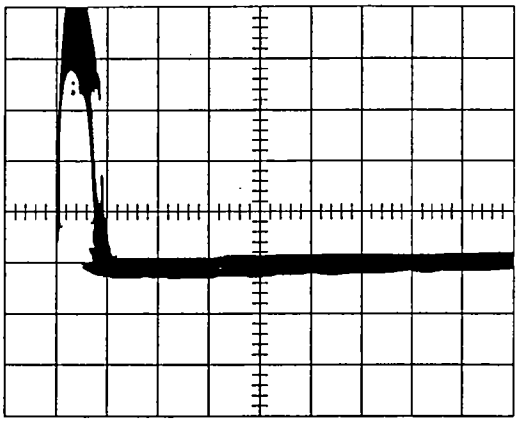


Figure B.1 Correct Pole/Zero Compensation

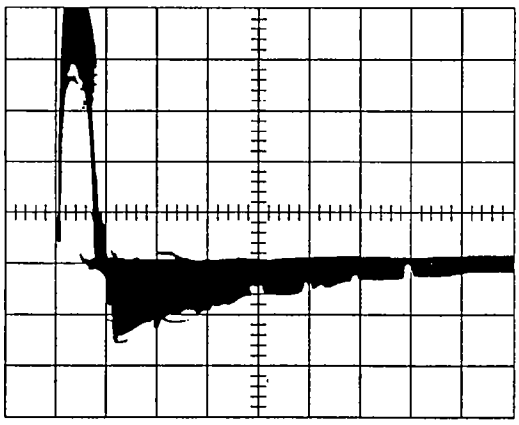
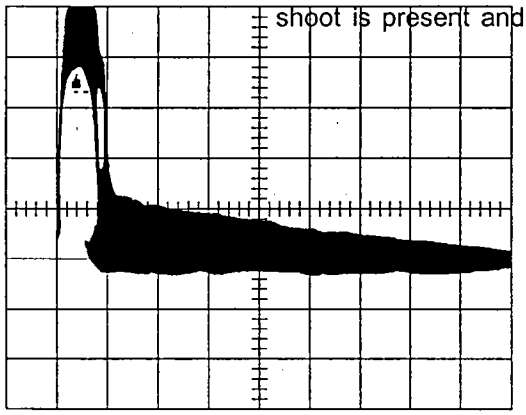


Figure B.2 Undercompensated Pole/Zero



shoot is present and is

Figure B.3 Overcompensated Pole/Zero

Scope
Vertical: 50 mV/division
Horizontal: 10 μs/division

Source $^{55}$Fe
5.9 keV peak: 7 V amplitude
Count rate: ≈ 2 kcps
Shaping: 2 μs

less than 20 mV, its impact on performance is insignificant. However, if small shaping undershoots are present, they should not be confused with preamp matching misadjustments undershoots, which exhibit a much longer time constant and have a larger performance impact. At high count rates, P/Z matching misadjustment will affect spectral peak shape and resolution.

## B.2 Pole/Zero Matching Using a Square Wave Generator

1. Driving a preamp test input with a square wave will allow a more precise adjustment of the pol/zero matching. The square wave signal must be of good quality with a flat top and bottom.

2. The amplifier's COARSE GAIN, SHAPING, and INPUT POLARITY controls should be set for the intended application.

3. Adjust the square wave generator for a frequency of approximately 1 kHz.
4. Connect the square wave generator's output to the Preamp's TEST INPUT.
5. Remove all radioactive sources from the vicinity if the Detector.
6. Using an oscilloscope, monitor the Model 2016's AMP OUT unipolar signal. Set the scope's vertical sensitivity to 5 V/div, and adjust the main time base to 0.2 ms/div. Adjust the square wave generator's amplitude control (attenuator) for a AMP OUT signal of 8 V.

Note Both positive and negative unipolar pulses will be observed at the output. Reduce the scope vertical sensitivity to 50 mV/div. To prevent scope overload, use a clamp box, such as the Canberra Model LB1502 Schottky Clamp Box, and set the CLAMP/DIRECT switch to CLAMP. With the unipolar signal clamped, adjust the P/Z control as illustrated in Figure B.4.

When adjusting the P/Z matching using the square wave technique, the calibration square wave generated by the oscilloscope can be used. Most scopes generate a 1 kHz square wave used to calibrate the vertical gain and probe compensation. Connect the scope Calibration Output through an attenuator to the preamp test input and perform the steps in this section again.

Figure B.4 shows the correct setting of the MANUAL P/Z control. Figures B.5 and B.6 show under- and overcompensation for the preamplifier decay time constant. As illustrated in Figure B.4, the unipolar output signal should have a clean baseline with no bumps, overshoots or undershoots.

## B.3 Baseline Restorer Mode

The baseline restorer in the Model 2016 is flexible in that both the symmetrical and asymmetrical modes are offered. In the SYMmetrical mode, the restoration currents are identical for above and below the baseline. For the asymmetrical mode, the restorer current above the baseline (referenced to the positive output), is much less than that below the baseline.

The symmetrical restorer mode is used on Ge systems with fast shaping and high count rates or with low quality preamps, for scintillation and proportional counting, and with Si systems.

The symmetrical mode should always be used for detector systems which exhibit baseline discontinuities resulting from excessive noise and/or high voltage effects, preamp reset pulses and preamp secondary time constants. Secondary preamp fall time constants result in unipolar output undershoots making it difficult to optimize the amplifier preamp matching.

The asymmetrical restorer mode offers superior high performance for high resolution Ge spectroscopy.

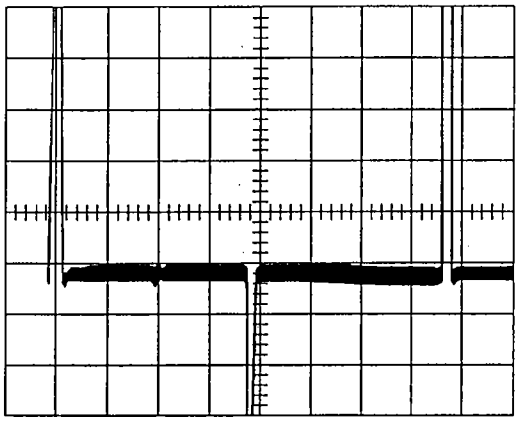


Figure B.4 Correct Pole/Zero Compensation

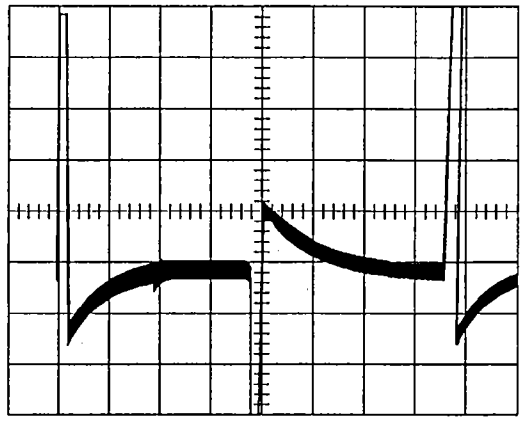


Figure B.5 Undercompensated Pole/Zero

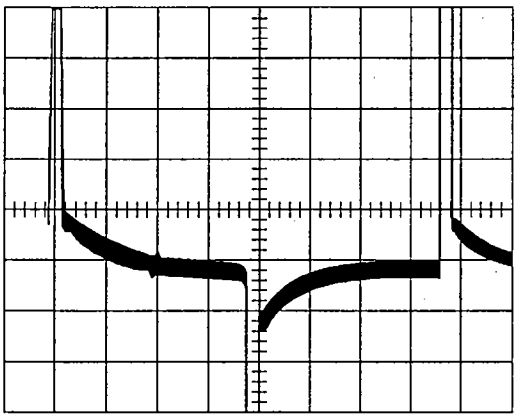


Figure B.6 Overcompensated Pole/Zero

Scope
Vertical: 50 mV/division
Horizontal: 50 µs/division

## B.4 Amplifier Shaping Selection

Shaping time constant selection generally is a compromise between optimizing throughput and resolution.

For germanium detectors, 4 µs shaping provides optimum resolution at low count rates, but 2 µs provides better performance over a wider range of count rates. For very high count rate applications the 2016A is recommended for its high throughput. For lower count rate and low energy applications, the 2016B is recommended for its better resolution.

For high resolution detectors, longer shaping time constants offer better signal to noise (S/N) ratio and reduced sensitivity to the effects of detector ballistic deficit. However, as the system count rate increases, resolution will degrade rapidly as a result of the amplifier's long processing time and the effects of pulse pile-up.

The optimum shaping time constant depends on the detector characteristics (such as size, noise characteristics, collection characteristics), preamplifier and incoming count rate. The 2016's shaping-time constant ranges for other common detectors are listed in the following table.

| Detector | Shaping (μs) |
|---|---|
| Scintillation Photomultiplier [NaI(Tl)] | 0.5, 1 |
| Planar Implanted Passive Silicon (PIPS) | 0.5, 1, 2 |
| Gas Proportional Counter | 0.5, 1, 2 |
| Lithium Drifted Silicon [Si(Li)] | 6, 12 |
| Lithium Drifted Germanium [Ge(Li)] | 2, 4 |
| Planar Germanium | 4, 6, 12 |
| Silicon Surface-Barrier (SSB) | 0.5 |
| Ultra-LEGe | 0.125, 0.25, 0.5 |
| Ge Array Detector | 0.125, 0.25, 0.5 |

Refer to the specific Detector Operator's Manual for the recommended shaping time. This will be a good starting point. Further refinements may be realized through experimentation. Collect spectra using shaping times above and below the recommended to find the one that provides optimal resolution performance for your particular detector and application.

Note The P/Z matching must be recalibrated each time the shaping is changed.

## B.5 Operation With Reset Preamps

The Model 2016 is fully compatible with most reset type preamps. These include the Model 2101 Transistor Reset Preamp, the Model 2008 Optical Reset Preamp, and the Model HRR High Rate Reset Preamp.

Reset preamps use an electronic circuit, as opposed to a feedback resistor to restore the preamp output back to a reference level. As a result, the reset preamp output is a succession of step functions that staircase or ramp up to an upper limit that initiates a preamp reset.

### B.5.1 P/Z Compensation With Reset Preamps

Since the reset preamp signal does not have the characteristic exponential fall time of RC preamps, pole/zero compensation is not required. When using the Model 2016 with a reset preamp, set the P/Z potentiometer to infinity, fully counterclockwise.

### B.5.2 Using the Reset Preamp Inhibit Signal

The preamp reset event produces a large signal, which drives the amplifier into a severe overload condition. The Model 2016 recovers from overload events rapidly and monotonically, requiring approximately two non-overload pulse widths to fully recover.

Converting events during amplifier overload may produce spectral distortion and it is recommended that the SCA and amplifier be gated OFF during this time using the preamp

INHIBIT signal. The preamp INHIBIT signal width should be adjusted to encompass the full unipolar signal recovery. The INHIBIT signal from the Model 2101 Transistor Reset Preamp, the Model 2008 Optical Reset Preamp or the Preamp Reset Module is positive true.

To properly make this adjustment:

1. Set the scope's vertical sensitivity to 20 mV/div.
2. Using a clamp box, such as the Canberra Model LB1502 Schottky Clamp Box, connect the Amp Out signal to one of the scope's inputs.
3. Connect the Inhibit signal to the scope's other input.
4. Trigger the scope on the leading edge of the Inhibit signal.
5. Adjust the width of the Inhibit signal so that it ends when the amplifier's output returns to within 2 mV of the baseline.

## B.6 Triangular Shaping

The peaking time for triangular shaping is approximately 14% longer than Gaussian shaping with an equivalent shaping time. The longer peaking time is equivalent to increasing the shaping time. This effectively increases the choice of shaping time constants from 6 to 12 when both shaping modes are considered.

The longer peaking time provides improved signal-to-noise ratio (SNR) and reduced electronic noise. Triangular shaping is also less sensitive to the effects of detector ballistic deficit. Both factors benefit by improved resolution performance. But you should be aware that the resolution improvement gained, due to the longer overall signal processing time, is at the expense of reduced maximum throughput.

## B.7 ICR Threshold Adjustment

Though the ICR threshold defaults to the automatic mode, in some cases you may want to set the ICR threshold manually. The ICR threshold must be set just above the system noise level to achieve optimum PUR performance. The ICR Auto Threshold Mode is enabled/disabled through a 2016 software switch.

1. Using the 2016 software, disable the PUR Auto Threshold setting.
2. Set the amplifier Gain and Shaping as required.
3. Remove all excitation sources from the vicinity of the Detector.

### B.7.1 Optimizing the Discriminator

This procedure optimizes the discriminator sensitivity to insure the threshold is at its lowest setting, just above the noise level.

1. Adjust the 2016 ICR THRESH control fully clockwise. The ICR RATE LED indicator is off.

2. Adjust the ICR RATE control counterclockwise until the ICR RATE LED indicator glows green continuously if the PUR is off, or red if the PUR is on.
3. Adjust the control clockwise until the indicator blinks occasionally.
4. The PUR threshold is now properly set.

Note With PUR Auto Threshold disabled, the PUR Threshold must be rechecked and adjusted if the Detector/Preamplifier or Amplifier's GAIN or SHAPING are changed.

## B.8 ADC Peak Detect Adjustment

Normally, the ADC will start its conversion when the peak of the input signal is detected. With the Delayed Peak Detect feature found in all Canberra ADCs, SCA calibration is greatly simplified because the peak value is held by the ADC's stretcher circuit until the end of the Delayed Peak period and allows the SCA's output to be used as a GATE input to the ADC. At high count rates, however, this extended ADC window will allow later and larger pulses to be partially captured; this can dull the apparent sharpness of the SCA's ULD cutoff. This is strictly an artifact of the ADC peak capture and is minimized by reducing the width of the Delayed Peak period.

To adjust the Delayed Peak period:

1. Select a source with moderate activity so that there are not a large number of piled up pulses.
2. Use the software to select an Amplifier/TCA. Its RDY LED will start blinking.
3. Select the amplifier's shaping time constant.
4. Set the pole/zero compensation.
5. Connect the ADC's Peak Detect INSPect test point to one of the scope's input.
6. Connect the selected SCA's Gate Input signal to the scope's other input.
7. Trigger the scope on the Peak Detect signal.
8. Adjust the Peak Detect signal's period so that it includes the SCA signal but does not go beyond it.

## B.9 Calibration and Normalization

Most Canberra ADCs are calibrated so that a 10 volt input will cause the ADC to convert near the channel selected for the Conversion Gain. For example, with a Conversion Gain of 2K, the ADC will nominally convert a full scale (+10 V) pulse at channel 2020 ±20 channels. But as the amplifier's pulse shaping is made faster, the ADC gain will drop and the 10 volt pulse will be converted at a lower channel. The 2016's circuits are better able to respond to amplifier shapes so that it is necessary to calibrate the MCA spectra to the SCA setting.

To make this adjustment:

1. Set the ADC's Peak Detect period as described in "ADC Peak Detect Adjustment" on page 37.
2. Using the software in the Calibration Mode, choose one of the available amplifiers.
3. Bring sources with known energy lines near the detector.
4. Set SCA windows to encompass these peaks. The individual SCAs in the module are enabled when their respective "Output Enable" is selected.
5. Adjust this amplifier's gain until these peaks are seen in the MCA spectrum. The RDY LED of the selected Amplifier/TCA will be blinking.
6. If all modules are to be set for the same energy range, TCA polarity, PUR, and Auto Threshold mode, select "Apply to all Amp/TCAs".
7. When the SCA calibration is complete, the MCA spectrum can then be calibrated. You must position the cursor on one peak centroid and select which SCA (1, 2 or 3) it corresponds to. This would normally be the highest energy peak.
8. Now calibration steps 3 through 6 can be repeated for the remaining Amplifier/TCA modules or, alternatively, to perform a Gain Normalization.
9. The Gain Normalization procedure uses the calibrated MCA and allows individual amplifiers to be selected and to manually adjust their Gain to position the spectrum at the proper locations. This will match the amplifier's gains to the calibrated module. The SCAs are forced to be at the widest limits and allow all pulses to be converted. Once again, the selected Amplifier/TCA will have its RDY LED blinking to aid in locating the amplifier to adjust.

# Request for Schematics

Schematics for this unit are available directly from Canberra. Write, call or FAX:

Training and Technical Services Department
Canberra Industries
800 Research Parkway, Meriden, CT 06450
Telephone: (800) 255-6370 or (203) 639-2467
FAX: (203) 235-1347

If you would like a set of schematics for this unit, please provide us with the following information.

Your Name _____

Your Address _____

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_____

Unit's model number _____

Unit's serial number _____

Note: Schematics are provided for information only; if you service or repair or try to service or repair this unit without Canberra's written permission you may void your warranty.

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This warranty covers Canberra hardware and software shipped to customers within the United States. For hardware and software shipped outside the United States, a similar warranty is provided by Canberra's local representative.

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Canberra warrants proper operation of its software only when used with software and hardware supplied by Canberra and warrants software media to be free from defects for 90 days from the date of shipment.

If defects are discovered within 90 days of the time you receive your order, Canberra will pay transportation costs. After the first 90 days, you will have to pay the transportation costs.

## LIMITATIONS

Upon notification of defects in the software media or hardware, Canberra will repair or replace the defective items at its discretion.

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