

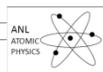
Combining Altera FPGAs With Arcturus μ C5282 Microcontrollers For Beamline Instrumentation At The APS

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Abstract
At the Advanced Photon Source (APS), we continue to combine the power and flexibility of Altera Field Programmable Gate Arrays (FPGA) with Arcturus μ C5282 embedded microcontrollers to provide low cost EPICS controlled solutions for beam line instrumentation.

In this paper, we discuss an application which couples an Altera Cyclone-II FPGA with an embedded Arcturus μ C5282 microcontroller to implement an instrument for a time-resolved, pump-probe timing experiment.



Instrument
The instrument, also referred to as the AMO Logic Gate, was developed for the XSD-AMO group and provides timing and logic functions. They probe laser modified molecules and atoms with x-rays, then use the instrument to separate the data taken with laser-on / laser-off conditions.

Input timing signals can be changed by specifying a delay and width in 5.68nS increments, and detector input signals can be divided-by N. Timing signals (Fig. 1) can be logically ANDed together to produce a GOOD output signal identifying a target bunch. All timing signals delays and widths, logical ANDing, and "divide-by" values are specified through an EPICS interface (Fig. 1 and Fig. 2).

Laser-on / laser-off is ANDed with GOOD and detector input signals to produce logic outputs (see Fig. 7 labelling). These conditions are dually output (isolated) at CMOS levels which can be connected to a scaler, oscilloscope, or beam line instrumentation.

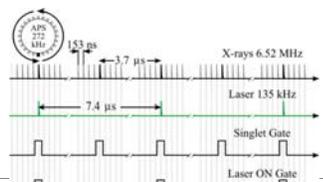


Fig. 1 (Courtesy of AMO Group)



Fig. 2



Fig. 3



Fig. 4



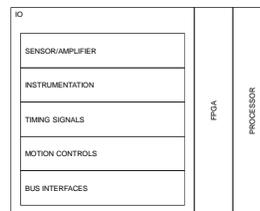
Fig. 5

Hardware Platform

Hardware is based on the "Generation II - Generic Digital" Cyclone-II FPGA board (Fig. 5). The μ C5282 is mounted on a carrier board that was developed at the APS. A daughter board was developed to accept the input signals from the APS timing system (P0) and from beam line instrumentation (NIM). Modified signals and logic functions are output which can be connected to external instrumentation. Divided input frequencies are output through a 50pin breakout module (Fig. 6). Users view timing signals and hardware status from a MEDM screen (Fig. 3). The FPGA base board, μ C5282 carrier, and daughter board are housed in a 2U rack mountable chassis (Fig. 8).

Development Concept

We continue to apply the "Generic Digital" concept to abstract the application behaviors and compartmentalize them, serving as our "design pattern." The model is described as below:



IO component represents the specific hardware designed for the particular needs of the application.

FPGA component includes in-house developed and commercial boards to handle the real-time aspects of the application.

PROCESSOR component typically uses the Arcturus μ C5282 microcontroller as an EPICS IOC running the RTEMS real time operating system. Alternatives are an EBRICK coupled with "Generation I - Generic Digital" hardware (Figs. 9, 10, 11), Altera NIOS-II soft-processor, or both a μ C5282 and NIOS-II.

Development Environment

Linux has the tools to develop EPICS, synApps, IOC, and hosts the RTEMS cross-compiler. Altera's Quartus-II software tool was used to develop the FPGA logic. Interaction between the μ C5282 and the FPGA is through the "bus bridge" that was developed here at the APS. It mediates data transactions and interrupt processing, and gives the application visibility to the functionality provided by the FPGA.

EPICS and synApps modules were based from the central repository shared by APS users, beamline scientists, and developers. The IOC application, configuration, data files reside on an APS server.



Fig. 8



Fig. 7



Fig. 6



Fig. 9



Fig. 10



Fig. 11



We would like to thank the AMO Group for the opportunity to work with them and for their support on this project. The Logic Gate has been a positive collaborative effort between the AMO and Detector development group.

The instrument has been used successfully during several runs at the APS. The next generation Logic Gate will employ the Stratix-II FPGA and have a resolution of <4nS.